In the Claims

Amend the Claims as follows:

1-5. (Previously Cancelled)

6. (Currently amended) A cache interface circuit, comprising:

a processor interface for receiving memory access requests from a processor, and for transmitting memory data back to said processor in response to processor requests;

a main memory interface for issuing main memory access requests to a main memory and for receiving main memory data in response;

a cache memory interface for issuing memory access requests to a cache memory, if operating in a cache mode, and for receiving cache memory data in response;

a cache-bypass mode-control signal input for said processor to indicate a cache bypass mode~~,~~ in response to a programmer instruction inserted in a program being executed by said processor explicitly for the purpose of switching to cache bypass mode, ~~a cache bypass mode~~ in which cache bypass mode memory access requests are serviced from said main memory;

a power control output for switching off operating power to said cache memory in response to a command received at said cache-bypass mode-control signal input that indicates all memory access requests should be serviced from said main memory.

7. (Original) The cache interface circuit of Claim 6, further comprising:

a cache-bypass mode program instruction interceptor connected to the processor interface and

providing for switching between said cache and cache-bypass modes without having received an explicit signal to do so at the cache-bypass mode-control signal input;

wherein, said processor need not take any action to switch between said cache and cache-bypass modes.

8. (Original) The cache interface circuit of Claim 7, further comprising:

a sequence of program instructions disposed in said main memory that require execution by said processor in said cache mode and that are bracketed by program instructions acted on by the cache-bypass mode program instruction interceptor to switch between said cache and cache-bypass modes.